

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

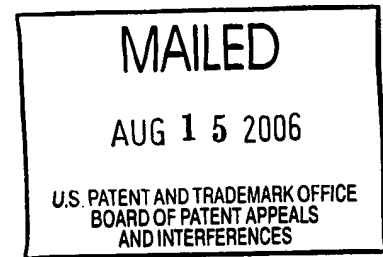
## UNITED STATES PATENT AND TRADEMARK OFFICE

### BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

*Ex parte* IAN MICHAEL HOLLAND and GARETH CHRISTOPHER MATTHEWS

Appeal No. 2006-0557  
Application No. 08/890,643

ON BRIEF



Before BARRY, BLANKENSHIP, and MacDONALD, *Administrative Patent Judges*.  
BARRY, *Administrative Patent Judge*.

A patent examiner rejected claims 1-27. The appellants appeal therefrom under 35 U.S.C. § 134(a). We reverse.

#### I. BACKGROUND

The invention at issue on appeal concerns memory-mapped input/output ("I/O") for a computer.<sup>1</sup> Memory-mapped I/O speeds the loading of data or code from storage into random access memory ("RAM"). Some computer operating systems, however, do

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<sup>1</sup>Figures showing the prior art shall "be designated by a legend such as 'Prior Art.'" M.P.E.P. § 608.02(g) (6th ed., rev. 2, July 1996). Here, Figure 1 of the appellants' specification "illustrates a **normal** memory-mapped file layout. . . ." (Spec., p. 5, l. 6 (emphasis added).) Similarly, Figure 4 of their specification "illustrates the process for a **standard** file I/O API operation." (*Id.*, p. 9, l. 16 (emphasis added).) Being "basically a board of review," *Ex parte Gambogi*, 62 USPQ2d 1209, 1211 (Bd.Pat.App. & Int. 2001), we leave the question of whether the Figures requires the aforementioned legend to the examiner and the appellants.

not support memory-mapped I/O. Using such operating systems to read large read-only files, complain the appellants, is slow and requires considerable disk space.

(Spec., p. 1, ll. 8-15.)

In contrast, the appellants' invention employs a converter program to create a simulated dynamic link library ("DLL"), which a system loader loads into a RAM. More specifically, data are wrapped with executable code, so that the loader treat, the data as a segment of code. To wit, when the corresponding virtual page is touched by a software application, the code is loaded. When the page grows old, it is discarded instead of being paged to a paging file. When the page is touched again, it is re-read from the original file like memory-mapped I/O. (*Id.*, p. 3, ll. 7-14.)

A further understanding of the invention can be achieved by reading the following claims.

1. A method comprising the steps of:

converting a read only file into an executable file; and  
memory-mapping the converted file into memory.

27. A method comprising the steps of:

converting a read-only file into a shared library with an executable code segment, wherein the shared library includes a reference pointer to data residing in the executable code segment;

an application that needs to use the data referencing a pointer to the data; and

an operating system faulting a page containing a memory segment wherein the read-only file resides into memory.

Claims 1-27 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,301,302 ("Blackard").

## II. OPINION

Our opinion addresses the claims in the following order:

- claims 1-26
- claim 27.

### A. CLAIMS 1-26

"Rather than reiterate the positions of the examiner or the appellants *in toto*, we focus on the point of contention therebetween." *Ex parte Muresan*, No. 2004-1621, 2005 WL 951659, at \*1 (Bd.Pat.App & Int. Feb 10, 2005). The examiner asserts, "The step of converting a read only file into an executable file is taught by the reference as the simulator copies data and instructions from Read Only Storage (ROS) into the operating system's shared memory segment. (See Col. 8 line 21 et seq.) The further step of memory mapping the converted file into memory is taught by the reference as

the memory mapping whereby addresses of a one segment of memory are mapped into a second segment of memory. (See Col. 16 line 21 et seq.)" (Examiner's Answer at 3.) The appellants argue, "*Blackard* does not teach that the BIOS copied from ROM is then memory-mapped." (Appeal Br. at 5.)

In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the independent claims at issue to determine their scope. Second, we determine whether the construed claims are anticipated.

### *1. Claim Construction*

"Analysis begins with a key legal question — *what is the invention claimed?*" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). Here, claim 1 recites in pertinent part the following limitations: "converting a read only file into an executable file; and memory-mapping the converted file into memory." Independent claims 7 and 13 recite similar limitations. Accordingly, claims 1, 7, and 13 require **initially** converting a read only file into an executable file and **subsequently** memory-mapping the converted file into memory.

## *2. Anticipation Determination*

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002).

"[A]n invention is anticipated if the same device, including all the claim limitations, is shown in a single prior art reference. Every element of the claimed invention must be literally present, arranged as in the claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed.Cir. 1989) (citing *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894, 221 USPQ 669, 673 (Fed. Cir. 1984); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771-72, 218 USPQ 781, 789 (Fed. Cir. 1983)). "[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Here, Blackard "relates to data processing systems running applications written for a specific first processor of a first processing system, and more particularly to a system and method of simulating the first processor for running the applications on a second processing system having a second dissimilar processor." (Col. 1, ll. 45-50.) The first passage of the reference cited by the examiner teaches translating a basic input/output system ("BIOS") into a file that can be executed to load a Disk Operating

System ("DOS"). (Col. 8, ll. 24-26.) The second passage cited by him teaches that "the memory of the first processing system must be mapped into the memory of the second processing system." (Col. 16, ll. 18-20.) We are unpersuaded, however, that Blackard initially converts the BIOS into the aforementioned executable file and then memory-maps the converted BIOS file into memory. To the contrary, the reference implies that memory-mapping is performed before translating. To wit, "[i]n order to translate the addresses of a first processing system into the addresses of a second processing system, the memory of the first processing system must be mapped into the memory of the second processing system." (*Id.* at ll. 16-20.)

The absence of initially converting a read only file into an executable file and subsequently memory-mapping the converted file into memory negates anticipation. Therefore, we reverse the rejection of claims 1, 7, and 13 and of claims 2-6, 8-12, and 12-26, which depend therefrom.

Before leaving claims 1-26, we note that the appellants cite to a specific page of a specific edition of the *Microsoft Press Computer Dictionary* in support of the novelty of claims 4, 10, and 16. (Appeal Br. at 6.) For our part, we found no copy of the page in the record. The appellants should ensure that copies of all evidence on which they rely are provided to the United States Patent and Trademark Office.

## B. CLAIM 27

The examiner alleges, "With respect to claim 27, the features of this claim are a restatement of the claimed elements already rejected." (Examiner's Answer at 6.) The appellants argue, "the Examiner has failed to specifically address the claim limitations within Claim 27, and as a result, the Examiner has failed to prove a *prima facie* case of anticipation in rejecting Claim 27." (Appeal Br. at 10.)

### 1. Claim Construction

"The Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582, 32 USPQ2d 1031, 1034 (Fed. Cir. 1994) (citing *In re Gulack*, 703 F.2d 1381, 1385, 217 USPQ 401, 403-04 (Fed. Cir. 1983)). Here, claim 27 recites in pertinent part the following limitations: "an operating system faulting a page containing a memory segment wherein the read-only file resides into memory."


### 2. Anticipation Determination


We agree with the appellant that the examiner has not addressed the aforementioned limitations, let alone show that these limitations are anticipated. Therefore, we reverse the rejection of claim 27.

### III. CONCLUSION


In summary, the rejection of claims 1-27 under § 102(e) is reversed.



  
LANCE LEONARD BARRY )  
Administrative Patent Judge )

  
HOWARD B. BLANKENSHIP  
Administrative Patent Judge

**HOWARD B. BLANKENSHIP**  
Administrative Patent Judge

  
ALLEN R. MacDonald  
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